CLAIMS

What is claimed is:

1. A memory system comprising:

a first plurality of memory cells, wherein each of the first plurality of memory cells includes a first node and a second node that are configured to have opposite logic values; and

a second plurality of memory cells, wherein each of the second plurality of memory cells includes a first node and a second node that are configured to have opposite logic values;

a first plurality of switches that are coupled the first nodes of the first plurality of memory cells;

a second plurality of switches that are coupled the second nodes of the second plurality of memory cells; and

wherein providing a pre-program data value to the first nodes of the first plurality of memory cells via the first plurality of switches, and to the second nodes of the second plurality of memory cells via the second plurality of switches enables the memory system to be pre-programmed.

2. The memory system of claim 1, further comprising a connection configured to provide a reprogram-data signal to the first nodes of the first and second plurality of memory cells, wherein the reprogram-data signal enables the memory system to be reprogrammed.

3. The memory system of claim 1, further comprising a connection configured to provide a reprogram-data signal to the second nodes of the first and second plurality of memory cells, wherein the reprogram-data signal enables the memory system to be reprogrammed.

4. The memory system of claim 1, further comprising a connection configured to provide a reprogram-data signal to the first nodes of the first and second plurality of memory cells, and an inverse of the reprogram-data signal to the second nodes of the first and second plurality of memory cells, wherein the reprogram-data signal and the inverse of the reprogram-data signal enable the memory system to be reprogrammed.

5. The memory system of claim 1, wherein the memory system is configured to output the logic values of the first nodes of the first and second plurality of memory cells.

6. The memory system of claim 1, wherein the memory system is configured to output the logic values of the second nodes of the first and second plurality of memory cells.

7. The memory system of claim 1, further comprising two-way inverting circuits coupled between respective first and second nodes of each of the first and second plurality of memory cells, wherein each of the two-way inverting circuits is configured to enable a respective first node to have an opposite logic value as a corresponding second node.

8. The memory system of claim 7, further comprising a first plurality of switches coupled to respective first nodes of the first plurality of memory cells, wherein each of the first plurality of switches is configured to provide a reprogram data signal to a respective first node responsive to a reprogram signal.

9. The memory system of claim 8, further comprising a second plurality of switches coupled to respective second nodes of the second plurality of memory cells, wherein each of the second plurality of switches is configured to provide an inverse of the reprogram data signal to a respective second node responsive to the reprogram signal.

10. A method for pre-programming a memory system having a first and second plurality of memory cells, wherein each of the first and second plurality of memory cells includes a first node and a second node, the method comprising:

providing a pre-program data value to the first nodes of the first plurality of memory cells via a first plurality of respective switches that are respectively coupled to the first nodes; and

providing the pre-program data value to the second nodes of the second plurality of memory cells via a second plurality of respective switches that are respectively coupled to the second nodes.

11. The method of claim 10, further comprising providing a reprogram-data signal to the first nodes of the first and second plurality of memory cells to enable the memory system to be reprogrammed.

12. The method of claim 10, further comprising providing a reprogram-data signal to the second nodes of the first and second plurality of memory cells to enable the memory system to be reprogrammed.

13. The method of claim 10, further comprising providing a reprogram-data signal to the first nodes of the first and second plurality of memory cells, and providing an inverse of the reprogram-data signal to the second nodes of the first and second plurality of memory cells to enable the memory system to be reprogrammed.

14. The method of claim 10, further comprising outputting the logic values of the first nodes of the first and second plurality of memory cells.

15. The method of claim 10, further comprising outputting the logic values of the second nodes of the first and second plurality of memory cells.

16. A pre-programmable memory system comprising:

a first and second plurality of memory cells, wherein each of the first and second plurality of memory cells includes a first node and a second node that are configured to have opposite logic values; and

means for providing a pre-program data value to the first nodes of the first plurality of memory cells via a first plurality of respective switches that are respectively coupled to the first nodes and to the second nodes of the second plurality of memory cells via a second plurality of respective switches that are respectively coupled to the second nodes.

17. The memory system of claim 16, further comprising:

means for providing a reprogram-data signal to the first nodes of the first and second plurality of memory cells to enable the memory system to be reprogrammed.

18. The memory system of claim 16, further comprising:

means for providing a reprogram-data signal to the second nodes of the first and second plurality of memory cells to enable the memory system to be reprogrammed.

19. The memory system of claim 16, further comprising:

means for providing a reprogram-data signal to the first nodes of the first and second plurality of memory cells, and providing an inverse of the reprogram-data signal to the second nodes of the first and second plurality of memory cells to enable the memory system to be reprogrammed.

20. The memory system of claim 16, further comprising:

means for outputting the logic values of the first nodes of the first and second plurality of memory cells.

21. The memory system of claim 16, further comprising:

means for outputting the logic values of the second nodes of the first and second plurality of memory cells.

22. A system for programming a memory system having a first and second plurality of memory cells, wherein each of the first and second plurality of memory cells includes a first node and a second node, the system comprising:

means for providing a pre-program data value to the first nodes of the first plurality of memory cells via a first plurality of respective switches that are respectively coupled to the first nodes; and

means for providing the pre-program data value to the second nodes of the second plurality of memory cells via a second plurality of respective switches that are respectively coupled to the second nodes.